# 2-YEAR M. TECH.
# IN
# COMPUTER APPLICATIONS

| I SEMESTER M.TECH - CA | | | | | |
|---|---|---|---|---|---|
| **Course No.** | **Name of the Courses** | **L** | **T** | **P** | **Credit Hrs.** |
| CSC51101 | Data Structure and Algorithms | 3 | 1 | 0 | **7** |
| CSC51102 | Digital Circuits and Computer Organization | 3 | 1 | 0 | **7** |
| CSC51103 | System Software | 3 | 1 | 0 | **7** |
| CSC51104 | Computer Graphics | 3 | 1 | 0 | **7** |
| CSC51105 | Programming Languages | 3 | 0 | 0 | **6** |
| CSC51206 | Data Structure and Algorithm Practical | 0 | 0 | 2 | **2** |
| CSC51207 | Digital Circuits and Comp. Organization Practical | 0 | 0 | 2 | **2** |
| CSC51208 | System Software Practical | 0 | 0 | 1 | **1** |
| CSC51209 | Computer Graphics Practical | 0 | 0 | 1 | **1** |
| CSC51210 | Programming Languages Practical | 0 | 0 | 2 | **2** |
| **Total** | | **15** | **2** | **8** | **42** |
| **Contact Hrs.** | | | | | **27** |

| CSC51102 | Digital Circuits and Computer Organization | 3-1-0 |
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**Number Systems and Codes:** Introduction, Data Representation, Number System Conversion, Complements, Integer/Floating Point Representation, Weighted and Un-weighted Codes, Alphanumeric Codes, Binary Addition, Binary Subtraction, Error Detection and Correction.
**Logic Gates:** Basic Gates, Universal Gates, Characteristics.
**Boolean Algebra:** Introduction, Booleans Rules and Laws, DeMorgan's Theorem, SOP and POS Form of Boolean Expressions, K-Map, Quine McCluskey Method)
**Combinational Circuits:** Introduction, Half/Full Adder, Half/Full Subtractor, Code Converter, Multiplexer, De-multiplexer, Encoder, Decoder.
**Sequential Circuits:** Introduction, Flip-Flops, Counters.
**Register Transfer and Micro-operations:** Register, Shift Register, Bus System (Multiplexer, Tri-State Buffer), Micro-operations (Arithmetic, Logic, Shift), Arithmetic Logic Shift Unit.
**Faster Algorithms:** Booth Algorithm and Bit-Pair Recoding Method for Signed Operand Multiplication, Restoring and Non-Restoring Integer Division Method.
**Basic Computer Organization and Design:** Process and Memory Interconnection, Instruction Codes, Instruction Cycle, Single-Bus Organization, Multiple Bus Organization, Addressing Modes.
**Control Unit:** Hardwired and Micro-programmed.
**Memory Organization:** Memory Hierarchy, Memory Types, Main Memory Architecture, Memory Address Map, Cache Memory, Virtual Memory, Paging, DMA.
**Input-Output Organization:** Introduction, I/O Versus Memory Bus, Asynchronous Data Transfer, Modes of Transfer (Programmed I/O, Interrupt-Initiated I/O, DMA).