Tanusree Kaibartta (Female, 32 Years)

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EDUCATIONAL QUALIFICATION

Doctor of Philosophy (PhD) in VLSI Testing (Pursuing)(2016 to till date)
IIT(ISM), Dhanbad, Jharkhand-826004, India
Thesis: Test strategies for VLSI designs including system on chip and 3D Integrated Circuits
Master of Science (M.E.) in Computer Science and Engineering with One Year Research Project **(2010 – 2012)**
Jadavpur University, India
Thesis:**Extraction of Vulnerability Information for Attack Graph Generation.**
CGPA: 7.75 out of 10
Bachelor of Technology (B.Tech.) in Computer Science and Engineering (Year: 2005 – 2009)
St. Thomas College of Engineering (Affiliated to WBUT)
DGPA: 8 out of 10

AWARDS & ACHIEVEMENTS

1. Qualified **West Bengal Joint Entrance Examination (WBJEE)** in 2005 conducted by **West Bengal Joint Entrance Examination Board.**
2. Qualified GATE (Graduate Aptitude Test in Engineering) in 2010.
3. Got placement in **TATA CONSULTANCY SERVICES** and worked approximately one year.
4. Qualified for the post of Assistant Professor (computer Science and Engineering) in 2013 conducted by **Indian School of Mines, Dhanbad, Jharkhand-826004, India.**

PROFESSIONAL EXPERIENCE

1. **RESEARCH EXPERIENCE:-**
    - 4 years of research experience in the field of VLSI Testing.
    - Participated Hands on training on **Synopsis and Xilinx.**

TEACHING EXPERIENCE

1. **Details of 5 years and 9 months (approx.) teaching experience.**

Sl. No.	Course Name	Batch	Strength	Session	Remarks
1.	Digital System Testing and Testable Design	B.Tech(8thSem)	103	2016-17	The course covers the topic of design for testing that adds testability features to a hardware product. Assignment based on Verilog and HOPE fault simulator.
2.	Computer Programming (Theory and Lab)	B.Tech (1stSem)	150 (Approx.)	2018-19(Odd) 2017-18(Even) 2016-17(Odd) 2015-16(Odd) 2014-15(Even) 2013-14(Odd)	The course is focused on C language programming.
3.	Formal Language and Automata Theory	B.Tech(Dual)	24 students	2016-17(even)	The course offers syntactical and semantic aspect of formal language. Apart from theoretical aspect, additional assignment based on current research work was given to students to enhance their knowledge.
4.	Object Oriented Programming (Theory and Lab)	B Tech (3rdSem)	190 (approx.)	2017-18(Odd 2016-17(Even)	The course mainly covers two object oriented language C++ and Basic JAVA. In template library of C++ and some of the advanced

				2015-16(Even)	topics of JAVA is covered. Lab work is performed on IDE Tools (Netbeans and eclipse).
5.	Software Engineering (Theory and Lab)	B.Tech(7thSem) B.Tech(5thSem)	194 150 (Approx.)	2018-19 (Odd) 2015-16(even) 2014-15(even)	Assignments are performed based on RSA Software tool.
6.	VLSI Design and Testing (Theory and Lab)	Btech Dual Degree (9thSem) M. Tech (2ndSem)	18(Approx.) 50(Approx.)	2018-19(Odd) 2014-15(Odd)	Introduction to the concepts and techniques of VLSI design, verification and testing, details of economy, fault modeling and simulation, Automatic Test Pattern Generation (ATPG), Built in self test etc.
7.	Digital System Testing and Testable Design	B.Tech(8thSem)	176 (Approx.)	2018-19(Even)	The course covers the topic of design for testing that adds testability features to a hardware product. Assignment based on Verilog and HOPE fault simulator.
8.	Computer Programming (Lab)	B.Tech (2nd Sem)	114	2018-19(Even)	The course is focused on C language programming.
9.	Database Management Systems (Theory and Lab)	B.Tech (8th Sem) Minor	28	2018-19(Even)	The course is focused on Database Management System concepts, Theoretical aspect of database which includes (UML, ER and Class Diagram, Relational Algebra, Relational Calculus, Indexing, Disk Storage) along with lab exercise on SQL query and Trigger on existing Database.

1. **Details of Research Guidance M. Tech.**

Sl. No.	Name of the student	Thesis title
1.	Mr. Abhisek Kumar	Compound Yield Optimization Technique For Wafer-to-Wafer 3D IC Integration.
2.	Mr. Sashank Srivastava	Increasing Fault Coverage Efficiency in Benchmark Circuits Using Design For Testability and Test Pattern Generation using Cellular Automata, Genetic Algorithm, Pseudorandom pattern Generation.
3.	Mr.Kunil Kumar	Test Time Optimization for Embedded Cores using ATE pattern Compression of Slice Data.
4.	Mr. Vikas Kumar Kisku	An Efficient Test Planning for Core-based 3D stacked ICs with Through Silicon Via under Power Constrains
5.	M. Swati Kumari	Test-wrapper optimization for embedded cores in through - silicon–via based three-dimensional system on chips
6.	Mr. Rajaram Chandra Shaw	Increasing Fault coverage Efficiency in Benchmark Circuits using Pseudorandom Test Generation by Cellular Automata and Genetic Algorithms.
7.	Mr. Ashish Gupta	Dynamic Thermal-Adaptive Routing for Network –On-Chip.
8.	Ms. Jayshree Beriha	Optimization of test architecture in 3dimensional stacked integrated circuits for session based and session less testing using hard system-on-chip.
9.	Ms. Sujata Sinha	Optimization of Core-based SOC test Scheduling with power constraint based on Particle Swarm Optimization Algorithm.
10.	Ms. Bidnashree Brahma	Optimization of test architecture in 3D Stacked integrated circuits.
11.	Mr. Rajnish Kumar	Cycle Accurate Power Model and Genetic 3D dimensional SOC test scheduling.
12.	Mr. Dheeraj Kumar Puskar	Dynamic Thermal-Aware Test Scheduling Based on On-Chip temperature sensors.
13.	Ms. Sukriti Poddar	Power Aware System on Chip Test Schedule Optimization Using Genetic Algorithm

RESEARCH GRANT

Sl. No.	Title of the project	Amount Sanctioned	Funding Agency	Remarks
1	Study and design of Test access mechanism for core based three dimensional SOCs	1,41,900 (Approx.)	TEQIP-II	Completed

PARTICIPATIONS

1. Participated on 3Days Workshop on Emerging and Post CMOS Technologies (**June 16-18, 2014**) sponsored by TEQIP II, Department of Information Technology, IIEST, Shibpur.
2. Participated and presented a paper in 16th IEEE Workshop on RTL and High Level Testing (**2015**) organized by IIT, Mumbai.
3. Participated in 29th International Conference on VLSI Design (**January 4-8, 2016**).
4. Attended lecture on Digital Microfluidic Biochips: From Manipulating Droplets to Quantitative Gene Expression Analysis (**11th August, 2016**) organized by Department of Computer Science, Jadavpur University.
5. Participated Winter school on optimization techniques organized by ACMU unit of ISI and IEEE CEDA (**December 15-20, 2016**).

PUBLICATIONS

1. T. Kaibartta, Chandan Giri, Hafizur Rahaman, Debesh K. Das, Optimizing test time for core-based 3-D integrated circuits by genetic algorithm, *Quality Electronic Design (ASQED), 6th Asia Symposium* , **Aug 4-5, 2015,** 112-117**.**
2. T. Kaibartta, Debesh K. Das, Testing of 3D IC with minimum power using genetic algorithm, *Design & Test Symposium(IDT), 10th International*, **Dec. 14-16, 2015**, 62-67.
3. T. Kaibartta, Debesh K. Das, Power Aware 3-D IC testing with Minimum Power using Genetic Algorithm, *16th IEEE Workshop on RTL and High Level Testing*, **Nov. 25-26**, **2015**.
4. T. Kaibartta, Debesh K. Das, Optimization of Test Wrapper for TSV based 3D SoC using Heuristic Approach, *9th IEEE International Workshop on Reliability Aware System Design and Test (RASDAT 2018)*, **Jan. 11, 2018**.
5. T. Kaibartta, Debesh K. Das, Optimization of Test Wrapper length for TSV based 3D SOCs using a heuristic approach, *VDAT*, **June 28- 30, 2018.**
6. T. Kaibartta, Debesh K. Das, Journal, An Approach of Genetic Algorithm for Power Aware Testing of 3D IC, IET Computers & Digital Techniques(in minor revision).
7. T. Kaibartta, G. P. Biswas, Sashank Shrivastava, Design of Hybrid Fault Simulator using Genetic Algorithm Based TPG, 2018, VLSID (Communicated).

FUTURE RESEARCH PLAN

Research Interest: Microfluidic Biochip, Cellular Automata, 3D IC.

TECHNICAL EXPERIENCE

1. Languages C, C++, HTML, JAVA, ASP, Verilog, MATLAB, LISP, Prolog.
2. IDE tools Eclipse, Netbeans, MySQL, SQL Serve, GNU for Artificial Intelligence.
3. IBM tool RSA, optimization tool CPLEX, LINGO.
4. Proficient in Latex, Microsoft Word, Microsoft Excel, Microsoft Power Point.

REFERENCES

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