Course Type	Course Code	Name of Course	L	T	P	Credit
DC2	MCC202	Computer Organization and Architecture	3	0	0	9

Course Objective
To impart an understanding of the internal organization and operations of a computer how it works, and how it interfaces to software etc. To introduce the concepts of processor logic design and control logic design.
Learning Outcomes
Upon successful completion of this course, students will understand to: ● Identify the basic structure and functional units of a digital computer ● Instruction set architecture ● Data representation and Computer Arithmetic ● Processor Design, pipelining and hazards ● Memory hierarchy and its organization ● I/O transfers and some initial basics of multi-core architectures.

Unit No.	Topics to be Covered	Lecture Hours	Learning Outcome
1	Functional units of a computer: CPU, memory, I/O; Instruction set architecture: Instruction format, addressing modes, ISAs for common CPUs and assembly languages	8	On successful covering these contents students will be able to understand functional unit of a computer, Instruction set architecture and assembly language.
2	Data representation: signed number representation, fixed and floating point representations; Computer arithmetic: Multiplication - shift-and-add, Booth multiplier etc, Division non-restoring and restoring techniques	9	These content will establish the understanding of data representation and basics of arithmetic operations being performed in computer.
3	Processor design: datapath components, control unit, pipelining and hazards	7	These content will enable the students to understand the concepts of CPU control unit design, concepts of pipelining and hazards.
4	Memory: concept of hierarchical memory organization, cache memory, mapping functions and replacement algorithms, main memory organisation, virtual memory	10	These content will establish the understanding of memory hierarchy and its organization along with concepts of mapping functions, replacement algorithms and virtual memory.
5	I/O transfers - program controlled, interrupt driven and DMA, I/O devices - secondary storage; Introduction to multi-core architectures	8	After successful coverage of these contents students will be able to understand I/O transfers and some initial basics of multi-core architectures.

Text Books:

1. D. A. Patterson, J. L. Hennessy, Computer Organization and Design, 5th Ed., Morgan Kaufmann, 2013.
2. W. Stallings, Computer Organization and Architecture: Designing for Performance, 9th Ed., Pearson, 2013.

Reference Books:

1. C. Hamacher, Z. Vranesic, S. Zaky, Computer Organization, 6th Edition, McGraw Hill Education, 2011.
2. M. Mano, Computer System Architecture, 3rd Ed., Pearson, 1992.