# Curriculum Vitae

## Personal Information


**Name:** **Rahul Bhattacharya**

**Date of birth:** **18th April, 1983**

**Nationality:** **Indian**

**Office Address:** **Department of Electronics Engineering,**
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## Objective

**Intend to build a career, committed and dedicated to state-of-the-art research and teaching in a hi-tech environment which helps me to explore myself fully and realize my potential.**

## Details of Employment

- From June 2013 to till date: **Assistant Professor**, Department of Electronics Engg., IIT(ISM) Dhanbad.
- From March, 2012 to May, 2013: **Senior Design Engineer** in High Speed Link Validation Group of Wireless Division in ST-Ericsson India Pvt. Ltd, Bangalore, India.
- From November, 2010 to March, 2012: **Senior Design Engineer** in High Speed Link Validation Group of Wireless Division in ST-Ericsson India Pvt. Ltd, Greater Noida, India.
- From August, 2006 to October, 2010: **Research Consultant** in Advanced VLSI Design Laboratory, IIT Kharagpur.
- From August, 2005 to August, 2006: **Project Engineer** in Semiconductor and Consumer Electronics Division in Wipro Technologies, Bangalore.

## Academic Qualifications

| Degree | Institution | Year | Discipline |
|---|---|---|---|
| **B.Tech** | NIT Durgapur | 2005 | Electronics & Communication Engg. |
| **MS (by Research)** | IIT Kharagpur | 2012 | Electrical Engineering |
| **Ph.D** | IIT(ISM) Dhanbad | 2019 | Electronics Engg.<br>Thesis title - *Emulation and Implementation of Behavioral Models of Some Analog and Mixed Signal Circuits on Field Programmable Gate Array (FPGA)* |

## Fields of Specialization

- Emulation friendly modeling of mixed-signal circuits.
- FPGA emulation of VLSI circuits.
- Evolutionary algorithms for test automation.
- Behavioral Modelling, CAD and testing of analog and mixed signal VLSI systems.
- High level fault modeling for analog circuits.
- Fault detection and diagnosis in VLSI circuits

## Teaching Experience

| Duration | Theory Courses | Laboratory Courses |
|---|---|---|
| **2013 to till date** | **UG:** Electronics Engineering, Power Electronics, Microelectronics and VLSI, Digital System Design using HDL | **UG:** Electronics Engineering Lab, Power Electronics Lab, VLSI Design Lab, Electronics Devices Lab. |
| | **PG:** VLSI Circuits Testing, CAD for VLSI, Test and Verification of VLSI Circuits | **PG:** Microelectronics and VLSI Lab, HDL based System Design Lab, Physical Design and EDA Lab |

## Research Projects

| Title of Project | Name of Sponsoring Organization | Duration | Amount (in Lakhs) | Role |
|---|---|---|---|---|
| Bandwidth Adaptive RF Power Amplifier Modeling for Cross Bandwidth Testing **(*Under ADI Innovation Fellowship Grant*)** | **Analog Devices India Pvt. Ltd. (ADI) Bangalore** | 1 year (from July 2024) | 4.0474 | PI |
| Emulation Friendly Modeling of RF Power Amplifier for Pre-Silicon Verification **(*Under ADI Innovation Fellowship Grant*)** | **Analog Devices India Pvt. Ltd. (ADI) Bangalore** | 1 year (from June 2023) | 4.72 | PI |
| Ultra-Low Power Neuromorphic Spiking Architecture for Assistive Smart Glasses | **MEITY, Govt. of India** | 5 years (from 2022 to 2027) | 86 | Co-PI |
| Test development of analog and mixed signal circuits by emulation and implementation of their behavioral models on FPGA | **IIT (ISM) Dhanbad (under *Faculty Research Scheme*)** | 3 years (from Feb,2015) | 7.91 | PI |
| Feasibility study on fault emulation of linear analog circuits on a programmable hardware | **IIT (ISM) Dhanbad (under the aegis of TEQIP-II)** | 6 months (from Nov, 2016) | 2.00 | PI |

## Special Awards/Honours Received

- **Awarded prizes and certificate of merit for 5th position in *All India Science Talent Examination*.**
- **Awarded *Peer to Peer Recognition* in ST-Ericsson India Pvt. Ltd. for successful establishment of simulation-based verification set up for LLI IOT.**

## Reviewer for

- **IEEE Transactions on Very Large-Scale Integration**
- **IEEE Access**
- **ICICA 2014 International Conference organized by NIT Durgapur**
- **Books by Cambridge University Press for undergraduate Electronics Engineering students.**

## *Membership of Professional Bodies*

1. **Member of IEEE**
2. **Member of VSI (VLSI Society of India).**

## *Declaration*

**I hereby state that the information furnished above is factually correct & true to the best of my knowledge.**