



**Indian Institute of Technology (ISM) Dhanbad**  
Office of the Dean (Research & Development)

|                                                                             |                                             |                         |
|-----------------------------------------------------------------------------|---------------------------------------------|-------------------------|
| Sanction No and Date:<br>ANRF/ECRG/2024/001084/ENS<br>Dated 27 August, 2026 | <b>IIT (ISM) Project No.</b><br>SRDP 1215 G | Date 17 September, 2026 |
|-----------------------------------------------------------------------------|---------------------------------------------|-------------------------|

**Advertisement for the position of Junior Research Fellow (JRF) under ANRF  
Prime Minister Early Career Research Grant Project**

Applications are invited under the sponsored project. The details of the project are as under:

|                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
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| <b>Position</b>                       | Junior Research Fellow                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Number of Position (s)</b>         | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Title of The Project</b>           | Cyber resilient wide area control of inverter-based power networks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>Principal Investigator</b>         | Dr. Priyatosh Mahish                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>Tenure of Project</b>              | Maximum three years or till the end of project, whichever is earlier.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Job Description</b>                | PSCAD/EMTDC simulation of cyber-physical networks in the large scale power systems. Hardware-In-Loop (HIL) validation of the simulation results.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Essential Qualification</b>        | First class B.E./B.Tech. in Electrical / Electrical & Electronics / Electrical & Instrumentation/Instrumentation & Control / Instrumentation Engineering or equivalent degree from a recognized University/Institute. Post graduate degree in Electrical Engineering with a specialization of Power system/Power electronics/Control systems, selected through a process described as any one of the following.<br>a. Scholars selected through National Eligibility Tests- CSIR-UGC NET (Assistant Professorship) and GATE<br>b. The selection process through National level examinations conducted by Central Government Departments and their Agencies and Institutions such as DST, DBT, DAE, DOS, DRDO, MoE, ICAR, ICMR, IIT, IISc, IISER, NISER etc. |
| <b>Desirable Qualification</b>        | Overall good academic record, sound analytical skills, and knowledge in PSCAD simulation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>Fellowship</b>                     | ₹ 37000+HRA@16% for first two years<br>₹ 42000+HRA@16% for third year<br>The HRA will be provided only for the non-availability of accommodation at the IIT(ISM) campus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>Last Date &amp; Time for Apply</b> | 30 <sup>th</sup> October 2026 & 5.00 PM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

(Signature of PI)

*Priyatosh Mahish*

The candidates who are interested to apply for the above post should send their CV (maximum 2MB) with complete information regarding educational qualification indicating percentage of marks/CGPA and divisions, details of work experience etc. **by email with IIT(ISM) Project Number on the subject line to Dr. Priyatosh Mahish at email id: priyatosh@iitism.ac.in** Shortlisted candidates will be informed on the date of interview. Mere possession of minimum qualification does not guarantee an invitation to the interview. Candidates will be shortlisted based on their merit and as per the requirement of the project. All candidates should make their own arrangements for their stay at Dhanbad, if required. No TA/DA will be paid to attend the interview.

(Signature of PI)

